

TABLE 1

20 Pin PDIP, SOIC	20 Pin SSOP	Name	Input Type	Pull-up/ Current Source	Output Type	Description
1	1	RA0	ST		N/A	Port Input
		AN0	AN		—	ADC Input
		OPA+	AN		—	Op Amp Non-inverting Input
2	2	RA1	ST		N/A	Port Input
		AN1	AN		—	ADC Input
		OPA-	AN		—	Op amp Inverting Input
7	7	RA2	ST		CMOS	Bi-directional I/O
		AN2	AN		—	ADC Input
		Vref2	AN			Voltage Reference Input for C2 Comparator
8	8	RA3	ST		CMOS	Bi-directional I/O
		AN3	AN		—	ADC Input
		Vref1	AN		—	Voltage Reference Input for C1 Comparator, ADC, and DAC Modules
3	3	RA4	ST		OD	Bi-directional I/O
		T0CK1	ST		—	T0 Clock Input
4	4	RA5	ST		—	Port Input
		MCLR	ST	No	—	Master Clear Input
		Vpp	Power		—	Programming Voltage
17	17	RA6	ST		CMOS	Bi-directional I/O
		OSC2	—		Xtal	Crystal/Resonator
		CLKOUT	—		CMOS	Internal Clock (Fosc/4) Output
18	18	RA7	ST		CMOS	Bi-directional I/O
		OSC1	Xtal		—	Crystal/Resonator
		CLKIN	ST		—	External Clock Input Connection.
		T1CK1	ST			Timer1 External Clock Input

20 Pin PDIP, SOIC	20 Pin SSOP	Name	Input Type	Pull-up/ Current Source	Output Type	Description
9	9	RB0	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		INT	ST		—	Interrupt
		AN4	AN		—	ADC, C1, or C2 Comparator Input
		VREF			AN	VREF Reference Output
10	10	RB1	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN5	AN		—	ADC, C1, or C2 Comparator Input
		VDAC			AN	DAC Output
19	19	RB2	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN6	AN		—	ADC, C1, or C2 Comparator Input
20	20	RB3	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN7	AN		—	ADC, C1, or C2 Comparator Input
		OPA			AN	Op Amp Output
11	11	RB4	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
12	12	RB5	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
13	13	RB6	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		PSMC1A			CMOS	PSMC1A Output
		C1			CMOS	C1 Comparator Output
14	14	RB7	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		PSMC1B			CMOS	PSMC1B Output
		C2			CMOS	C2 comparator Output
		T1G	ST		—	Timer1 Gate Input
16	16	Vdd	Power		—	Digital Power
5	5	Vss	Power		—	Digital Ground
15	15	AVdd	Power		—	Analog Power
6	6	AVss	Power		—	Analog Ground

Legend: ST=Schmitt Trigger Input Voltage Levels, CMOS=Complimentary Metal Oxide Semiconductor Output Voltage Levels, TTL=Transistor Transistor Logic Input Voltage Levels, AN=Analog I/O Voltage Levels, OD=Open Drain Output, Xtal=Crystal, RBPU=Port B Pull-Up

TABLE 2A

Alternate Function	PORTA (when not in digital I/O)							
	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
Low Leakage Input only	—	—	—	—	—	—	< 60pA (tested to 50nA)	< 60pA (tested to 50nA)
ADC	—	—	—	—	AN3	AN2	AN1	AN0
Op Amp	—	—	—	—	—	—	OPA- Input	OPA+ Input
VREF Inputs	—	—	—	—	VREF2 Input	VREF1 Input	—	—
Timer0	—	—	—	T0CKI	—	—	—	—
Timer1	T1CKI	—	—	—	—	—	—	—
Oscillator	OSC1/CLKIN	OSC2/CLKOUT	—	—	—	—	—	—
Reset	—	—	MCLR	—	—	—	—	—
Programming	—	—	Vpp	—	—	—	—	—

**Note 1:** Dashed cell implies that the Alternate Function does not apply.

TABLE 2B

Alternate Function	PORTB (when not in digital I/O)							
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
INT	—	—	—	—	—	—	—	INT
ADC	—	—	—	—	AN7	AN6	AN5	AN4
Op amp	—	—	—	—	OPA Output	—	—	—
C2 comparator	C2 Output	—	—	—	AN7	AN6	AN5	AN4
C1 comparator	—	C1 Output	—	—	AN7	AN6	AN5	AN4
VREF Reference	—	—	—	—	—	—	—	VREF Output
DAC	—	—	—	—	—	—	—	VDAC Output
PSMC	PSMC1B Output	PSMC1A Output	—	—	—	—	—	—
Timer1	T1G Input	—	—	—	—	—	—	—
Programming	Data	Clock	—	—	—	—	—	—

**Note 1:** Dashed cell implies that the Alternate Function does not apply.

TABLE 3

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RA0/AN0/OPA+, RA1/AN1/OPA-	<p>DATA BUS</p> <p>WR ANSEL</p> <p>RD PORT</p> <p>ANSEL Latch</p> <p>Data Latch</p> <p>Schmitt Trigger</p> <p>To Analog to Digital Converter, and Op Amp Input</p>
RA2/AN2/VREF2 AND RA3/AN3/VREF1	<p>DATA BUS</p> <p>WR PORT</p> <p>WR TRIS</p> <p>RD TRIS</p> <p>WR ANSEL</p> <p>RD PORT</p> <p>Data Latch</p> <p>TRIS Latch</p> <p>ANSEL Latch</p> <p>Data Latch</p> <p>Schmitt Trigger</p> <p>To Analog to Digital Converter and VREF1 or VREF2 input</p>

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RA4/T0CKI	
RA5/MCLR/Vpp	

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RA6/OSC2/CLKOUT	<p>Block circuitry for RA6/OSC2/CLKOUT pin. The circuit includes a Data Latch, TRIS Latch, and RD PORTA. It features an oscillator circuit connected to the pin, which can be configured as an output (CLKOUT) or an input (INTRC or RC with CLKOUT). The output is driven by a PMOS transistor (P) and pulled down by an NMOS transistor (N). A Schmitt Trigger Input Buffer is also shown.</p>
RA7/OSC1/CLKIN	<p>Block circuitry for RA7/OSC1/CLKIN pin. The circuit includes a Data Latch, TRIS Latch, and RD PORTA. It features an oscillator circuit connected to the pin, which can be configured as an input (CLKIN) or an output (INTRC or RC with CLKOUT). The output is driven by a PMOS transistor (P) and pulled down by an NMOS transistor (N). A Schmitt Trigger Input Buffer is also shown.</p>

TABLE 3 (cont'd)

PIN NAME

EXEMPLARY BLOCK CIRCUITRY

RB0/INT/AN4/VREF

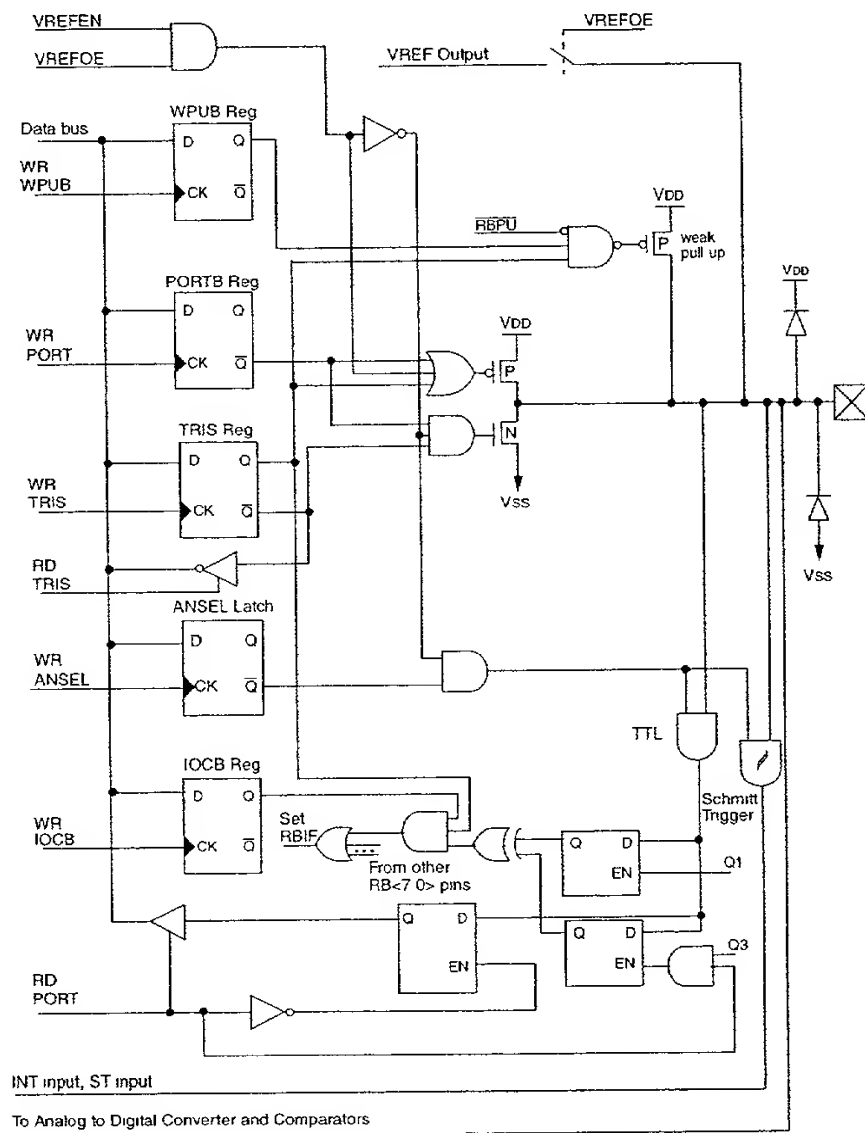


TABLE 3 (cont'd)

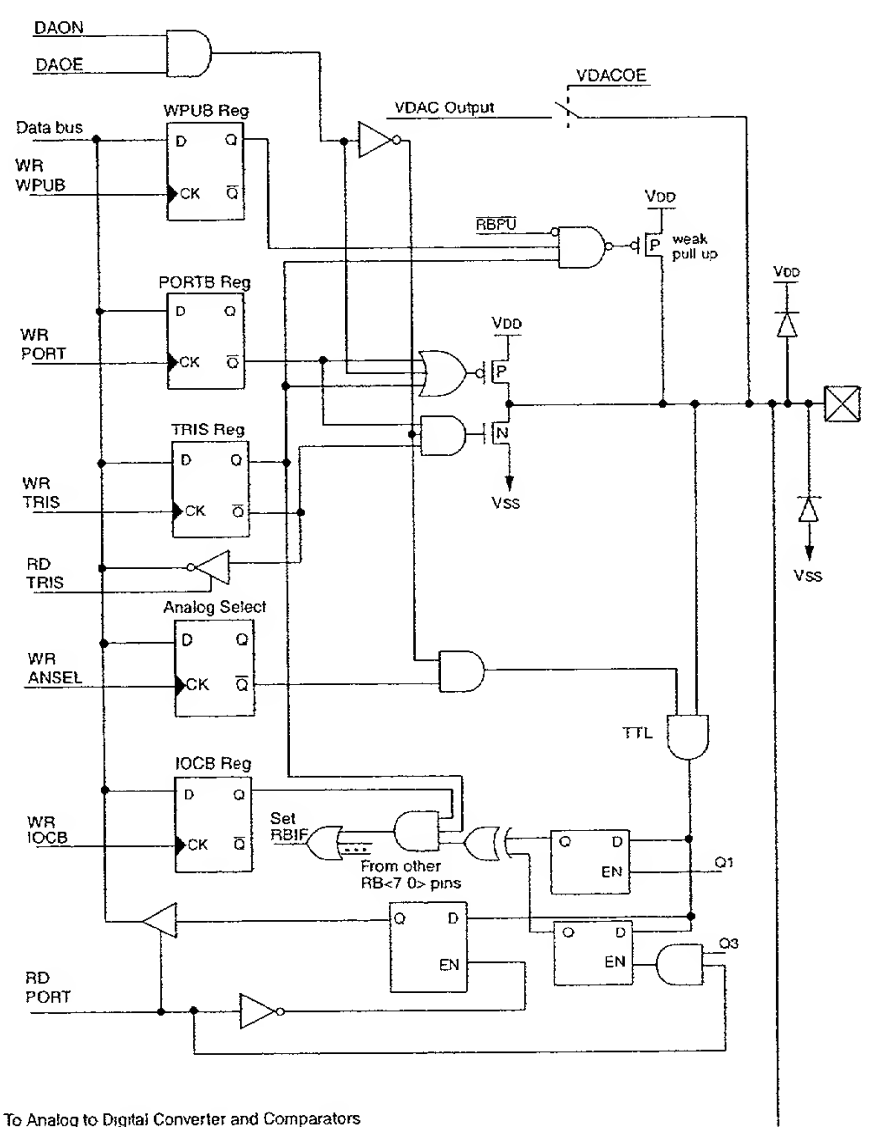
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB1/AN5/VDAC</p>	 <p>To Analog to Digital Converter and Comparators</p>



TABLE 3 (cont'd)

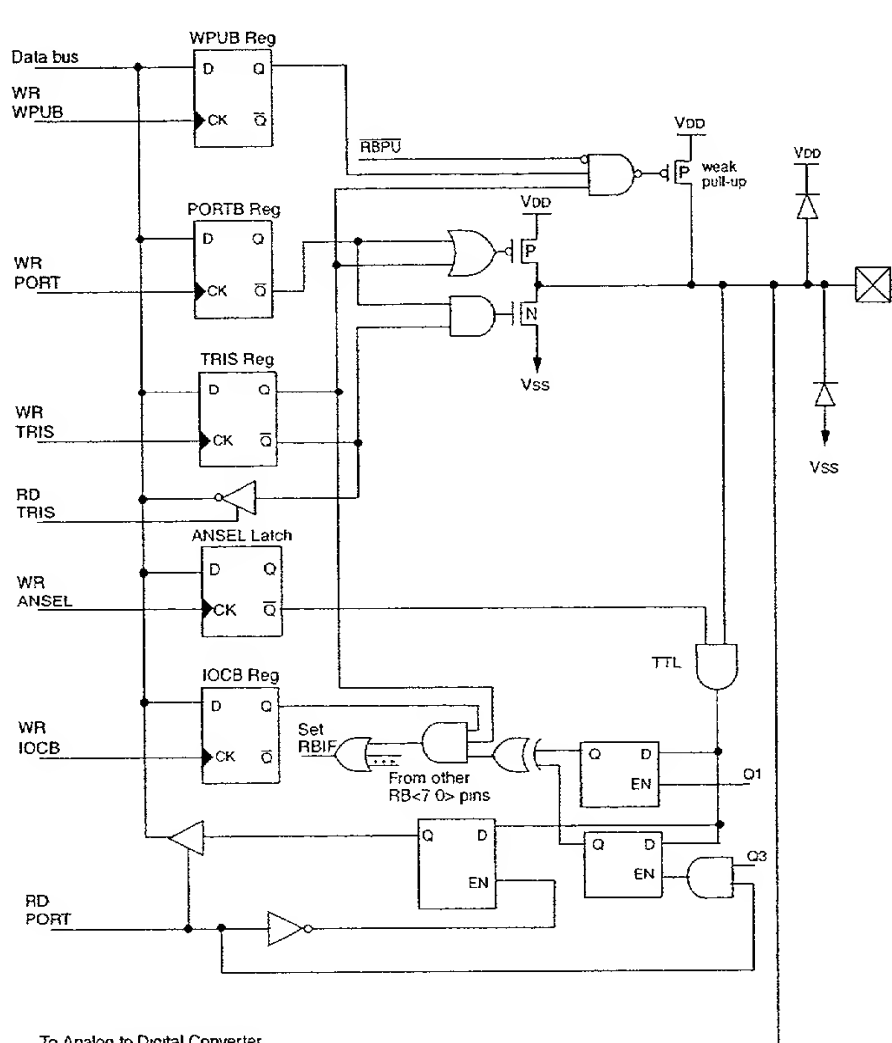
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB2/AN6</p>	 <p>The circuit diagram for pin RB2/AN6 illustrates the internal logic of the microcontroller. It features several registers and latches connected to the Data bus and control signals (WR, RD, WPUB, PORT, TRIS, ANSEL, IOCB). The WPUB Reg (Weak Pull-Up Register) controls a weak pull-up transistor connected to VDD. The PORTB Reg (Port B Register) and TRIS Reg (Tri-State Register) control the output driver transistors (PMOS and NMOS) connected to VDD and VSS. The ANSEL Latch (Analog Select Latch) controls the connection of the pin to the internal circuitry. The IOCB Reg (IO Control Register) controls the connection of the pin to the internal circuitry. The circuit also includes a Set RBIF (Set Port B Interrupt Flag) signal, a TTL (Transistor-Transistor Logic) input, and a connection to the Analog to Digital Converter (ADC) via a multiplexer (Q1, Q2, Q3).</p>

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RB3/AN7/OPA	<p>The diagram for RB3/AN7/OPA shows the internal logic of the pin. It includes registers for WPUB, PORTB, TRIS, ANSEL, and IOCB. The output is connected to an Op Amp Output through a weak pull-up resistor (RBP) and a diode to VDD. The circuit also includes a TTL input and a diode to VSS.</p>
RB4 AND RB5	<p>The diagram for RB4 AND RB5 shows the internal logic of the pins. It includes registers for WPUB, PORTB, TRIS, and IOCB. The output is connected to a weak pull-up resistor (RBP) and a diode to VDD. The circuit also includes a TTL input and a diode to VSS.</p>

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB6/C1/PSMC1A</p>	<p>The diagram illustrates the internal block circuitry for the RB6/C1/PSMC1A pin. It shows the connection of various control signals to the pin's internal logic, including the Data bus, WR WPUB, WR PORTB, WR TRISB, RD TRISB, and WR IOCB. The circuit includes several registers (WPUB Reg, Data Latch, TRIS Latch, RD PORTB, IOCB Reg) and latches. A weak pull-up resistor (RBPU) is connected to VDD. The input signal is buffered by a TTL input buffer and a Schmitt Trigger. The output is connected to a TTL output buffer (Q1) and a Schmitt Trigger (Q3). The circuit is controlled by a Serial Programming Clock and a Set RBIF signal.</p>

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB7/C2/PSMC1B/T1G</p>	<p>The diagram illustrates the internal block circuitry for the pin RB7/C2/PSMC1B/T1G. Key components and connections include:</p> <ul style="list-style-type: none"> <li><b>Registers and Latches:</b> WPUB Reg, IOCB Reg, Data Latch, and TRIS Latch are connected to the Data bus and control signals (WR, RD, I/O).</li> <li><b>Control Signals:</b> SMCON, SMCOM, SCS, C2OE, RBPV, VDD, and VSS are shown as inputs or outputs.</li> <li><b>Logic and Buffers:</b> The circuit includes various logic gates (AND, OR, NOT), a Schmitt Trigger, and a TTL input buffer.</li> <li><b>Output and Input:</b> The pin output is connected to Q1 and Q3, which are also connected to the RD Port. A weak pull-up is connected to VDD.</li> <li><b>Other Connections:</b> The circuit is connected to the Data bus, WR, RD, and I/O signals, and a Serial programming input and Timer1.</li> </ul>